

Zhewen Pan

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Education

University of Wisconsin-Madison , Electrical and Computer Engineering <i>PhD</i>	2022 - Present
· Advisor: Joshua San Miguel · Research interest: Efficient Architectures and Systems	
University of Wisconsin-Madison , Electrical and Computer Engineering <i>Master of Science in Computer Engineering, GPA: 3.94/4</i>	2020 - 2022
· Relevant coursework: Computer Architecture, Operating Systems, Compilers, High Performance Computing.	
Purdue University , Electrical and Computer Engineering <i>Bachelor of Science with Highest Distinction, GPA: 3.99/4</i>	2016 - 2020
· Relevant coursework: Computer Organization, DNNs, Statistical Machine Learning.	

Awards & Honors

Google PhD Fellowship	2025
Rising Stars in EECS, MIT&BU	2025
Sarah and David Epstein Teaching Fellow, UW-Madison College of Engineering	2025
Best Paper Honorable Mention, ISCA	2025
IEEE Micro Top Picks Honorable Mention	2025
First Place, Google "Sustainability for AI Datacenters" N+1 Institute Reverse Pitch Competition Scholarship	2024
Department of ECE Gerald Holdridge Teaching Excellence Award, UW-Madison	2024
Distinguished Artifact Award, ASPLOS	2024
Second Place, ACM Student Research Competition (SRC) Grand Finals Grad Division	2023
Gold Medal, ACM Student Research Competition (SRC) SIGMICRO Grad Division	2023
gem5 Boot Camp Travel Grant	2022
ISCA Student Travel Grant	2022
Wisconsin Distinguished Graduate Fellowship - Schneider	2022

Publications – Conferences

- Zhewen Pan, Joshua San Miguel. **The XOR Cache: A Catalyst for Compression**. *International Symposium on Computer Architecture (ISCA)*, 2025. [paper]. 🏆 **Best Paper Honorable Mention**.
- Zhewen Pan, Joshua San Miguel, Di Wu. **Carat: Unlocking Value-Level Parallelism in GEMMs**. *ACM Conference on Architectural Support for Programming Languages and Operating Systems (ASPLOS)*, 2024. [paper]. 🏆 **IEEE Micro Top Picks 2025 Honorable Mention & 🏆 Distinguished Artifact Award**
- Di Wu, Jingjie Li, Zhewen Pan, Younghyun Kim, Joshua San Miguel. **uBrain: A Unary Brain Computer Interface**. *International Symposium on Computer Architecture (ISCA)*, 2022. [paper].

Publications – Workshops

- Zhewen Pan, Joshua San Miguel. **The XOR Cache: A Catalyst for Compression**. *ACM Student Research Competition (SRC) Co-located w/ MICRO*, 2023. 🏆 **The ACM SRC 2023 SIGMICRO gold medal & grand finals second place**
- Zhewen Pan, Di Wu, Joshua San Miguel. **T-MAC: Temporal Multiplication with Accumulation**. *The 4th Young Architect Workshop (YArch) Co-located w/ ASPLOS*, 2022.

Research

Harnessing Fault Tolerance for Sustainability	Oct 2024 - Present
· Characterizing memory failure patterns over time and developing models to estimate carbon emissions from aging hardware.	

- Mapping error-tolerant data to aging memory cells to extend hardware lifetime and reduce embodied carbon.

 Google "Sustainability for AI Datacenters" N+1 Institute Reverse Pitch Competition Scholarship, first place

XOR Cache: A Catalyst for Compression

Sep 2022 - Nov 2024

- Identified cross-level value redundancy in caches and reframed it as an opportunity for compression.
- Designed a compressed cache that co-locates similar lines using XOR pairing, enhancing compressibility and therefore efficiency.

Carat: Unlocking Value-Level Parallelism in GEMMs

Dec 2021 - Mar 2023

- Introduced value-level parallelism to reduce redundant computation by processing only unique input values in AI workloads.
- Designed a GEMM accelerator that reuses results via temporal subscription and value delivery for efficient execution.

uBrain: Unary Computing Brain Computer Interface

Oct 2021 - Mar 2022

- Designed and synthesized unary hardware modules and performed regression analysis on efficiency statistics.

Scalable Deadlock-Freedom Network-on-Chip

Jan 2021 - May 2021

- Characterized deadlock criticality based on the impact of positive feedback loops between congestion and deadlock formation.
- Proposed and evaluated a scalable subtractive deadlock-removal scheme based on packet bypassing using gem5-Garnet.

Employment

Arm Inc

May 2021 - Aug 2021

System IP Interconnect Performance Modeling Intern

Austin, TX (Remote)

- Developed a test suite for Coherent Mesh Interconnect performance modeling flow and evaluated associated tooling.

Professional Service

ISCA Undergrad Architecture Workshop (uArch) Mentor

2023, 2025

MICRO Artifact Evaluation Program Committee

2022

Teaching

Teaching Assistant, UW-Madison, ECE/CS 552: Introduction to Computer Architecture

Fall 23, Spring 24, Spring 25, Fall 25

Teaching Assistant, UW-Madison, ECE 554: Digital Engineering Laboratory

Spring 22

Teaching Assistant, Purdue, ECE 270: Digital System Design

Spring 20

Teaching Assistant, Purdue, ECE 362: Microprocessor Systems and Interfacing

Spring 19

Teaching Assistant, Purdue, ECE 270: Digital System Design

Spring 18

Teaching Assistant, Purdue, ENGR 131: Transforming Ideas to Innovation I

Fall 17