Zhewen Pan

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Education

University of Wisconsin-Madison Sep 2022 - May 2027 (Expected)
PhD

- Electrical and Computer Engineering
- Advisor: Joshua San Miguel
- Research interests: Novel Architectures and Systems

University of Wisconsin-Madison Sep 2020 - May 2022
Master of Science in Computer Engineering

- Electrical and Computer Engineering

Purdue University Aug 2016 - May 2020
Bachelor of Science in Electrical Engineering with Highest Distinction

- Electrical and Computer Engineering

Publications – Conferences

Zhewen Pan, Joshua San Miguel. **The XOR Cache: A Catalyst for Compression**. *International Symposium on Computer Architecture (ISCA)*, 2025. 🏆 Best Paper Nominee

Zhewen Pan, Joshua San Miguel, Di Wu. **Carat: Unlocking Value-Level Parallelism in GEMMs**. *ACM Conference on Architectural Support for Programming Languages and Operating Systems (ASPLOS)*, 2024. 🏆 IEEE Micro Top Picks 2025 Honorable Mention 🏆 Distinguished Artifact Award

Di Wu, Jingjie Li, Zhewen Pan, Younghyun Kim, Joshua San Miguel. **uBrain: A Unary Brain Computer Interface**. *International Symposium on Computer Architecture (ISCA)*, 2022.

Publications – Workshops

Zhewen Pan, Joshua San Miguel. **The XOR Cache: A Catalyst for Compression**. *ACM Student Research Competition (SRC) Co-located w/ MICRO*, 2023. 🏆 The ACM SRC 2023 SIGMICRO gold medal and grand finals 2nd place

Zhewen Pan, Di Wu, Joshua San Miguel. **T-MAC: Temporal Multiplication with Accumulation**. *The 4th Young Architect Workshop (YArch) Co-located w/ ASPLOS*, 2022.

Research

Taming Memory Errors for Sustainable Computing Oct 2024 - Present

- Characterizing time-dependent memory aging-induced failure profile.
- Mapping fault tolerance data to failed memory cells for further amortizing embodied emission.

🏆 N+1 Institute Google Reverse Pitch Competition 1st place scholarship

XOR Cache: A Catalyst for Compression Sep 2022 - Nov 2024

- Characterized synergy between reversible transformations and prior cache compression schemes to boost compression ratio.
- Modeling the proposed compression scheme and cache coherence protocol in gem5 Ruby.

Carat: Unlocking Value-Level Parallelism in GEMMs Dec 2021 - Mar 2023

- Implemented scheduling for the proposed temporal computing architecture in our in-house performance modeling platform
- Evaluated hardware efficiency through event-based power/energy modeling framework.

uBrain: Unary Computing Brain Computer Interface Oct 2021 - Mar 2022

- Designed and synthesized hardware modules and performed regression analysis on efficiency statistics

Scalable Deadlock-Freedom Network-on-Chip Jan 2021 - May 2021

- Characterized deadlock criticality based on impact of positive feedback loop between congestion and deadlock formation
- Proposed and evaluated a scalable subactive deadlock-removal scheme based on packet bypassing using gem5-Garnet

Awards and Honors

ISCA Best Paper Award Nominee (XOR Cache)	2025
IEEE Micro Top Picks Honorable Mention (Carat)	2025
N+1 Institute Google Reverse Pitch Competition 1st place scholarship	2024
Department of ECE Gerald Holdridge Teaching Excellence Award	2024
Distinguished Artifact Award (Carat)	2024
Second Place in the ACM Student Research Competition (SRC) Grand Finals Grad Division	2023
Gold Medal in the ACM SIGMICRO Student Research Competition (SRC) Grad Division	2023
gem5 Boot Camp Travel Grant	2022
ISCA Student Travel Grant	2022
Wisconsin Distinguished Graduate Fellowship - Schneider	2022

Employment

Arm Inc May 2021 - Aug 2021
System IP Interconnect Performance Modeling Intern *Austin, TX (Remote)*

- Designed Out-of-the-Box test suite for Coherent Mesh Interconnect performance modeling flow, covering topology, traffic profile, runtime options, system address map variations
- Performed ad-hoc testing on performance application user interface and provided feedback

Projects

Implementation of MLP-aware Cache Replacement Policy Madison, WI

- Implemented the MLP-aware LIN cache replacement policy in gem5 simulator
- Simulated and evaluated performance on the SPEC2006 CPU benchmark suite compiled for the x86 ISA
- Performed sensitivity analysis w.r.t varying L2 cache configuration and level of reordering aggressiveness

Dual-Core Coherent MIPS Processor Datapath and Memory System Design West Lafayette, IN

- Designed a 5-stage pipelined datapath with forwarding, and a 2-layer dynamic adaptive branch predictor
- Developed a coherent cache hierarchy implementing a snooping-based protocol
- Implemented lock-based synchronization hardware support in the multicore system to enforce write atomicity
- Verified design in gate-level simulation and prototyped the synthesized design on Altera FPGA

Professional Service

ISCA Undergrad Architecture Workshop (uArch) Mentor	2023, 2025
MICRO Artifact Evaluation Program Committee	2022

Teaching

ECE/CS 552: Introduction to Computer Architecture	Fall 2023, Spring 2024, Spring 2025
ECE 554: Digital Engineering Laboratory	Spring 2022
ECE 270: Digital System Design	Spring 2020
ECE 362: Microprocessor Systems and Interfacing	Spring 2019
ECE 270: Digital System Design	Spring 2018
ENGR 131: Transforming Ideas to Innovation I	Fall 2017

Skills

Programming Languages	C, C++, Python, SystemVerilog, Verilog
Tools	gem5, Quartus, Modelsim, Altium, OpenRoad
Languages	Chinese (native), English (fluent), Japanese (beginner)